IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

#30

In Re Application of:

Melik Isbara

Serial No. 08/925,868

Filed: September 9, 1997) Examiner: Wells, K.

For: METHOD AND APPARATUS FOR INTERFACING MIXED VOLTAGE SIGNALS) Art Unit: 2816

Honorable Commissioner of
Patents and Trademarks
Washington, D.C. 20231

APPEAL BRIEF
IN SUPPORT OF APPELLANT'S APPEAL
TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Members of the Board:

Appellant (hereafter "Appellant") hereby submits this Brief in triplicate in support of his Appeal from a final decision by the Examiner in the above-captioned case. Appellant respectfully requests consideration of this Appeal by the Board of Patent Appeals and Interferences for allowance of the claims in the above-captioned patent application.

An oral hearing is not desired.

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

The invention is assigned to Intel Corp, a Delaware corporation with headquarters in Santa Clara, California.

II. RELATED APPEALS AND INTERFERENCES

To the best of Appellants' knowledge, there are no appeals or interferences related to the present appeal which will directly affect, be directly affected by, or have a bearing on the Board's decision.

III. STATUS OF THE CLAIMS

Claims 1-17,19, and 20 are currently pending in the above-referenced patent application. Claims 1-17,19, and 20 were rejected in a Final Office Action mailed on October 12, 2000.

In the Office Action mailed June 20, 2000, claims 1-17, 19 and 20 are rejected under 35 U.S.C. 103 as obvious in light of any one of Fox, U.S. Patent No. 3,579,023 (henceforth Fox), Nelson, U.S. Patent No. 4,507,618 (henceforth Nelson), and GB 1,287,021 (henceforth GB). Claims 1, 8, 13, 15, and 17 (the independent claims) are the subject of this appeal.

IV. STATUS OF AMENDMENTS

In response to the Final Office Action mailed on October 12, 2000 in which all claims were rejected, Appellants timely filed a Notice of Appeal on November 7, 2000.

A copy of the claims 1,8, 13, 15, and 17 which are the subject of this appeal are attached hereto as Appendix A.

V. SUMMARY OF THE INVENTION

More and more digital systems are designed to operate at mixed voltage levels. Thus, some circuits of a system may operate at first binary signal levels, and others in the system may operate at second binary signal levels. A problem arises when interfacing circuits operating at the different signal levels. Prior art voltage level shifters have introduced substantial propagation delays when converting a binary signal between voltage levels, resulting in reduced performance of the overall system.

Claims 1,8, 13, 15, and 17 ("the claims") recite a specific application of an electronic circuit configuration for the purpose of converting a binary input signal with a first two levels to a binary output signal with a second two levels. The claims are directed to reducing the undesirable effects of prior art binary level shifters.

The claims recite an apparatus and method involving a biased transistor. The transistor comprises a parasitic capacitance that cooperates with a resistive element coupled to the transistor's enable terminal. Such cooperation acts to increase the voltage applied to the

transistor's enable terminal (typically the gate terminal) during the transition of a binary signal at the input terminal from a first to a second binary voltage levels. In other words, the transistor exhibits voltage "pumping" at the enable terminal to affect the impedance between the input and output terminals during a transition from the first to the second binary levels at the input terminal. Such pumping action enhances the signal propagation from input to output terminals, reducing propagation delays.

VI. ISSUES PRESENTED

1. Whether the claimed invention is structurally equivalent to known R-C attenuator circuits.

2. Whether the claims merely recite "field of use" restrictions of known R-C attenuator circuits.

3. Whether rejection of a process claim (such as claim 15) as merely reciting a "field of use" restriction is appropriate.

VII. GROUPING OF CLAIMS

For the purposes of this appeal:

Claims 1, 8, 13 and 17 stand or fall together as Group I.

Claim 15 stands or falls together as Group II.

Reasons for patentability of the above indicated claim groups are presented in the argument section pursuant to 37 C.F.R. §1.192(c)(5).

VIII. ARGUMENT

A) REJECTION OF CLAIMS 1-17 AND 19-20 UNDER 35 U.S.C. 103(A) AS OBVIOUS IN LIGHT OF ANY ONE OF FOX, NELSON, AND GB IS IMPROPER. THE CLAIMED INVENTION IS NOT STRUCTURALLY EQUIVALENT TO THE RC ATTENTUATOR CIRCUITS TAUGHT BY THE REFERENCES.

1. Claim Group I

To sustain a rejection under 35. U.S.C. 103(a), the cited reference must teach or render obvious all elements of the claims. The Applicant and the Examiner agree that each reference teaches (in various fashion) one or more RC attenuator circuits. However, contrary to the assertions in the Examiner, the claims of Group I do not recite an RC attenuator. The transistor recited in the claims is not, as the Examiner maintains, merely acting in substitution of a discrete resistor in parallel with the capacitor of an RC attenuator. It is true that a transistor, continuously biased ON, may provide impedance between its input and output terminals, e.g. resistance. However, unlike a discrete resistor, the transistor comprises a parasitic capacitance that cooperates with a resistive element coupled to the transistor's enable terminal. Such cooperation acts to increase the voltage applied to the transistor's enable terminal (typically the gate terminal) during the transition of a binary signal at the input terminal from a first to a second binary voltage level. In other words, unlike a discrete resistor, the transistor exhibits voltage "pumping"

at the enable terminal to affect the impedance between the input and output terminals during a transition from the first to the second preselected voltage level at the input terminal.

In fact, such "pumping" action is contrary to the "attenuation" produced by an RC attenuator, in that the effect of such pumping actually enhances signal propagation from input to output terminals. Attenuation, by contrast, involves the inhibition of signal propagation between terminals.

It is facially apparent that the claimed circuit, comprising among other things a biased transistor comprising a parasitic capacitance, is not structurally equivalent to an RC attenuator circuit comprising a discrete resistor. Nor is the transistor of the claims a mere resistive replacement for the discrete transistor of an RC attenuator. As already noted, the transistor contributes far more than a mere resistance between its terminals. Thus, it would not be obvious, as the Examiner asserts, to merely replace the resistor in an RC attenuator circuits of Fox, Nelson, or GB with a continuously biased transistor to accomplish the claimed invention.

B) REJECTION OF CLAIMS 1-17 AND 19-20 UNDER 35 U.S.C. 103(A) AS OBVIOUS IN LIGHT OF ANY ONE OF FOX, NELSON, AND GB IS IMPROPER. THE CLAIMED INVENTION IS NOT A MERE "FIELD OF USE" RESTRICTION OF A KNOWN RC ATTENUATOR CIRCUIT.

1. Claim Group I

MPEP 2111.02 states:

THE INTENDED USE MAY FURTHER LIMIT THE CLAIM IF IT DOES MORE THAN MERELY STATE PURPOSE OR INTENDED USE

Intended use recitations and other types of functional language cannot be entirely disregarded. However, in apparatus; article, and composition claims, intended use must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. In re Casey, 370 F.2d 576, 152 USPQ 235 (CCPA 1967); In re Otto, 312 F.2d 937, 938, 136 USPQ 458, 459 (CCPA 1963) (The claims were directed to a core member for hair curlers and a process of making a core member for hair curlers. Court held that the intended use of hair curling was of no significance to the structure and process of making.)

Respectfully, as noted in Argument A, the cited prior art and the claimed invention are not structurally the same, nor are they even structurally similar. One comprises discrete resistor, the other comprises a biased transistor with parasitic capacitance. The Examiner asserts that the Applicant may not argue functional differences when the prior art shows the identical structure, but the Examiner continues to rely upon prior art with substantially different structure to support this assertion. In other words, the Examiner asserts that Applicant is really claiming an RC attentuator, despite the fact that the claimed circuit operates differently (using charge pumping), with a different effect (level shifting of a binary signal), using a different structure (a biased transistor instead of a discrete resistor). According to the MPEP:

Intended use recitations and other types of functional language cannot

be entirely disregarded.

Hence both structural and functional limitations must be considered when interpreting the novelty of apparatus claims.

However, in apparatus, article, and composition claims, intended use must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art.

It is facially apparent that an RC attenuator has different structure than the claimed circuit. The RC attenuators taught by the cited references cannot level shift a binary signal using charge pumping. The claimed circuit utilizes a biased transistor with parasitic capacitance for this purpose. Thus, the structural differences (e.g. use of the biased transistor) arise from the intended use (e.g. level shifting a binary signal using charge pumping).

If the prior art structure is capable of performing the intended use, then it meets the claim.

The prior art RC attenuator is incapable of performing the intended use, namely, to provide level shifting of a binary signal by way of a pumping action as provided by the biased transistor. Thus it does not meet the claims. The claimed circuit comprises both a different function (e.g. pumping), and structural differences (e.g. the use of a biased transistor) arising from what the Examiner asserts is an intended use (the couplings to particular signal sources and sinks).

C) REJECTION OF CLAIMS 15 AND 16 UNDER 35 U.S.C. 103(A) AS OBVIOUS IN LIGHT OF ANY ONE OF FOX, NELSON, AND GB IS IMPROPER. THE CLAIMED METHOD IS NOT A MERE "FIELD OF USE" RESTRICTION OF A KNOWN RC ATTENUATOR CIRCUIT, AND FURTHER, "FIELD OF USE" IS AN INAPPROPRIATE BASIS FOR REJECTION OF PROCESS CLAIMS OF THE TYPE PRESENTED.

1. Claim Group II

Applicant asserts that it is inappropriate to rely upon the "field of use" or "intended use" doctrine in rejection of process claims, unless the claims are drawn to a process of manufacture (see MPEP 2111.02). There is no basis in examination practice or case law for a "field of use" rejection of process claims not drawn to a process of manufacture. Assuming, arguendo, that the claimed structure is known in the art, it is long established that novel uses, even those involving well-known structures, are inherently patentable. Furthermore, the cited references do not even teach the structures of the apparatus claims (see Arguments A and B, above), and furthermore, the process claims are not specific to the structure of the apparatus claims, but rather stand on their own functional limitations.

IX. CONCLUSION

Appellants respectfully submit that all the pending claims in this patent application are patentable and request that the Board of Patent Appeals and Interferences overrule the Examiner and direct allowance of the rejected claims.

This brief is submitted in triplicate, along with a check for $310.00 to cover the appeal fee for one other than a small entity as specified in 37 C.F.R. § 1.17(c). Please charge any shortages and credit any overcharges to Deposit Account No. 02-2666.

Respectfully submitted,

Date: 1-05-2001

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X. APPENDIX A: CLAIMS ON APPEAL

1. An apparatus comprising:

a transistor having an enable terminal, an input terminal, and an output terminal, said input terminal coupled to receive binary signals that vary between first and second preselected voltage levels, and said output terminal coupled to deliver binary signals that vary between the first preselected voltage level and a third preselected voltage level;

a capacitor coupled across said input and output terminals of said transistor; and

a resistive element having a first end portion coupled to the enable terminal of said transistor and a second end portion coupled to a voltage supply to bias the transistor continuously on, the resistive element cooperating with a parasitic capacitor defined by said transistor to increase the voltage applied to the enable terminal during a transition from the first to the second preselected voltage level at the input terminal.

8. An apparatus for converting first digital signals that vary between a first and second preselected voltage levels to second digital signals that vary between the first and a third preselected voltage level, comprising:

a pass gate transistor having a gate, source, and drain, said drain coupled to to receive said first signals, said source coupled to deliver said second signals, said gate coupled to a voltage supply;

a capacitor coupled across said source and drain of said pass gate transistor; and

a pump coupled to the gate of said pass gate transistor, said pump being configured to increase the voltage level applied to said gate during a transition from the first to the second preselected voltage levels.

13. An apparatus for converting an input signal that varies between first and second preselected voltage levels to an output signal that varies between the first preselected voltage level and a third preselected voltage level, comprising:

a first circuit;

a pass gate transistor having a gate, source, and drain, said drain coupled to receive said input signal, said source coupled to deliver said output signal, said gate being coupled to a voltage supply;

a capacitor coupled across said source and drain of said pass gate transistor; and

means for increasing the voltage level applied to said gate during a transition of the input signal from the first to the second preselected voltage level.

17. A buffer circuit, comprising:

a pass gate transistor having a gate, source, and drain, said drain coupled to receive a first digital signal that varies between first and second voltage levels;

a first voltage supply coupled to the gate of said pass gate transistor to bias the transistor continuously on;

a capacitor coupled across the source and drain of said pass gate transistor;

an inverter having an input terminal and an output terminal, said input terminal coupled to the source of said pass gate transistor to receive a second digital signal that varies between the first voltage level and a third voltage level;

a pull-up transistor having a source coupled to a second voltage supply, a drain coupled to the source of said pass gate transistor, and a gate coupled to the output terminal of said inverter; and

a resistive element coupled between said first voltage supply and the gate of said pass gate transistor, the resistive element cooperating with a parasitic capacitor defined by the drain and gate of said pass gate transistor to increase the applied voltage to the gate of said pass gate transistor.

AF/2876

PTO/SB/21 (12/97)
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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application No.	08/925,868
Filing Date	September 9, 1997
First Named Inventor	Melik Isbara
Group Art Unit	2816
Examiner Name	Wells, K.
Attorney Docket Number	42390P4537

Total Number of Pages in This Submission

ENCLOSURES *(check all that apply)*

- ☒ Fee Transmittal Form
  - ☒ Fee Attached
- ☐ Amendment / Response
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Assignment Papers *(for an Application)*
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition Routing Slip (PTO/SB/69) and Accompanying Petition
- ☐ To Convert a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Small Entity Statement
- ☐ Request for Refund
- ☐ After Allowance Communication to Group
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☒ Appeal Communication to Group *(Appeal Notice, Brief, Reply Brief)*
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Additional Enclosure(s) *(please identify below):*
  - Appeal Brief in triplicate
  - Check for $310.00
  - Return Receipt Postcard

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Paul A. Mendonsa, Reg. No. 42,879 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	Paul A Mendonsa
Date	January 5, 2001

CERTIFICATE OF MAILING/TRANSMISSION

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FEE TRANSMITTAL for FY 2000

Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT ($) 310.00

Complete if Known	
Application No.	08/925,868
Filing Date	September 9, 1997
First Named Inventor	Melik Isbara
Examiner Name	Wells, K.
Group/Art Unit	2816
Attorney Docket Number	42390P4537

METHOD OF PAYMENT (check one)

1. ☒ The Commissioner is hereby authorized to credit any overpayments to:

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Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

☒ Charge Any Additional Fee(s) Required Under 37 CFR §§ 1.16,1.17, 1.18 and 1.20.

☐ Applicant claims small entity status. See 37 CFR 1.27.

2. ☒ **Payment Enclosed:**

☒ Check ☐ Credit card ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	710	201	355	Utility filing fee	
106	320	206	160	Design filing fee	
107	490	207	245	Plant filing fee	
108	710	208	355	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES

	Extra Claims		Fee from below	Fee Paid
Total Claims	-	=	X	=
Independent Claims	-	=	X	=
Multiple Dependent				

**or number previously paid, if greater, For Reissues, see below

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	80	202	40	Independent claims in excess of 3
104	260	204	135	Multiple Dependent claim, if not paid
109	80	209	40	**Reissue independent claims over original patent
110	18	210	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

FEE CALCULATION (continued)

3. ADDITIONAL FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	*Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	*Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for response within first month	
116	390	216	195	Extension for response within second month	
117	890	217	445	Extension for response within third month	
118	1,390	218	695	Extension for response within fourth month	
128	1,890	228	945	Extension for response within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	310.00
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,240	241	620	Petition to revive - unintentional	
142	1,240	242	620	Utility issue fee (or reissue)	
143	440	243	220	Design issue fee	
144	600	244	300	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	130	123	130	Petitions related to provisional applications	
126	180	126	180	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	710	246	355	Filing a submission after final rejection (37 CFR 1.129(a))	
149	710	249	355	For each additional invention to be examined (37 CFR 1.129(b))	
179	710	279	355	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	

Other fee (specify) _____

Other fee (specify) _____

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SUBTOTAL (3) ($) 310.00

SUBMITTED BY

Complete (if applicable)

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